UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/539,314	06/15/2005	Johannus Wilhelmus Weekamp	NI 021492	2479

24737 7590 02/13/2007

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
SINGAL, ANKUSH K	
ART UNIT	PAPER NUMBER
2823	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/539,314	WEEKAMP ET AL.	
	Examiner	Art Unit	
	Ankush k. Singal	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
    (1) Field of the Invention.
    (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-3,5,6,7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lorentz et al.(US 6,324,072) in view of Nakatani et al(US PGPub 2002/0117743)

Re. Claim 1, Lorentz et al. discloses an electronic device comprising the steps of: providing a substrate having a substrate (same as first layer of an electro conductive material)(3), in which layer patterns are defined in accordance with desired pattern;

providing a foil having a second substrate (same as second patterned layer of electro conductive material), in which layer conductors are defined in accordance with a desired pattern;

Providing elements, include semiconductor chips (same as semiconductor elements) and a first conductor track plane (same as first connection element)(3) on the first side of the substrate, thereby bringing the first conductor track plane (same as first connection element)(3) and conductors in the first layer into electric contact; and also establish a electric contact between the second conductor track planes (same as second connection element)(6) and the corresponding conductors in the second layer(5).

Lorentz et al. does not teach having the encapsulation and separating the assembly of substrate.

However, Nakatani et al teaches separating the assembly of substrate and encapsulation as can be seen in figure 7H.

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Lorentz et al. in view of Nakatani et al. to separate the assembly of substrate to repair bad components on the release layer (same as assembly of substrate) and to encapsulate the elements to manufacture the semiconductor device.

Re. Claim 2, Lorentz et al. disclose all the limitations except removing the detachable layer.
However, Nakatani et al. discloses removing the release carrier (710)(same as detachable layer).
It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Lorentz et al. in view of Nakatani et al. to remove the detachable layer to coat the organic film.

Re. Claim 3, Lorentz et al. discloses a foil comprising a second substrate (same as patterned layer)(5) and the foil are provided in such a manner that the second patterned layer faces the elements (Figure 1). It is apparent to have the foil comprising a electrically isolating layer otherwise the device will be short circuited.

Re. Claim 5, Lorentz et al. disclose all the limitations except having the connection conductors already defined in the first layer.

However, Nakatani et al. teaches having the wiring patterns (same as connection conductor) defined in the first layer (701)(figure 7A).

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Lorentz et al. in view of Nakatani et al. to have the connection conductors already defined in the first layer to have better thermal stress.

Re. Claim 6, Lorentz et al. disclose all the limitations except removing the sacrificial layer.
However, Nakatani et al. discloses removing the release carrier(710)(same as sacrificial layer) after the provision of passivating material. It is apparent to undergo the provision of passivating material to encapsulate the elements.
It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Lorentz et al. in view of Nakatani et al. to remove the sacrificial layer to manufacture the semiconductor device.

Re. Claim 7, Lorentz et al. does not teach having the encapsulation.

However, Nakatani et al teaches encapsulation of the sheet material (same as second patterned layer) and that the substrate has contact faces (709) for external contacting are situated on the second side facing the first side and can be seen in figure 7I.

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Lorentz et al. in view of Nakatani et al. to separate the assembly of substrate to repair bad components on the release layer (same as assembly of substrate) and to encapsulate the elements to manufacture the semiconductor device.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lorentz et al.(US 6,324,072) in view of Nakatani et al(US PGPub 2002/0117743) as applied to claim 1 and further in view of Dubin et al(US 4,897,327).

Re. Claim 4, Lorentz et al. discloses the foil provided in such a manner that the second patterned layer faces the elements (Figure 1).

Lorentz et al. does not teach having a electrically isolating gauze.

However, Dubin et teaches having a fiber glass board(same as electrically isolating gauze).

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Lorentz et al. in view of Nakatani et al. and Dubin et al. to have a electrically isolating gauze to make integrated circuit boards.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lorentz et al.(US 6,324,072) in view of Nakatani et al(US PGPub 2002/0117743).

Re. Claim 8, Lorentz et al. discloses a electronic device comprising the steps of:

providing a substrate having a substrate (same as first layer of an electro conductive material)(3), in which layer patterns are defined in accordance with desired pattern;

providing a foil having a second substrate (same as second patterned layer of electro conductive material), in which layer conductors are defined in accordance with a desired pattern;

Providing elements, include semiconductor chips(same as semiconductor elements) and a first conductor track plane(same as first connection element)(3) on the first side of the substrate, thereby bringing the first conductor track plane(same as first connection element)(3) and conductors in the first layer into electric contact; and also establish a electric contact between the second conductor track planes(same as second connection element)(6) and the corresponding conductors in the second layer(5).

Lorentz et al. does not teach having the encapsulation.

However, Nakatani et al teaches encapsulation as can be seen in figure 7H.

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Lorentz et al. in view of Nakatani et al. to encapsulate the elements to manufacture the semiconductor device.

Re. Claim 9, Lorentz et al. discloses the second substrate (same as second conductive layer) on the side facing away from the elements. It is apparent to

have the foil comprising a patterned isolating layer otherwise the device will be short-circuited.

Re. Claim 11, Lorentz discloses a foil comprising a patterned. electrically conductive layer. It is apparent to have the foil comprising a patterned isolating layer otherwise the device will be short-circuited and it is also apparent that the layers have different patterns.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lorentz et al.(US 6,324,072) in view of Nakatani et al(US PGPub 2002/0117743) as applied to claim8 and further in view of Dubin et al(US 4,897,327).
Re. Claim 10, Lorentz et al. discloses all the limitations as discussed in claim 8, but does not teach having gauze of isolating material.
However, Dubin et teaches having a fiber glass board(same as isolating gauze).
It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Lorentz et al. in view of Nakatani et al. and Dubin et al. to have a gauze of isolating material to make integrated circuit boards.

Re. Claim 12, Lorentz et al. discloses the foil provided in such a manner that the second patterned layer faces the elements (Figure 1).
Lorentz et al. does not teach the isolating carrier layer is a gauze.

However, Dubin et teaches having a fiber glass board(same as isolating carrier layer is a gauze).

It would have been obvious for one with ordinary skill in the art at the time the invention was made to modify Lorentz et al. in view of Nakatani et al. and Dubin et al. to have the isolating carrier layer being a gauze to make integrated circuit boards.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ankush k. Singal whose telephone number is 5712701204. The examiner can normally be reached on monday-friday 7am-5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MATTHEW SMITH can be reached on (571)272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ankush Singal

LEX MALSAWMA
PRIMARY PATENT EXAMINER